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Paper No. 18

Application Number: 09/881,675
Filing Date: June 18, 2001
Appellant(s): ISHIMURA ET AL.

Gregory J. Maier
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07-31-2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

The amendment after final rejection filed on 03-31-03 has been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-3 and 5, claim 4, claims 6-8 and 10, and claim 9 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,229,166	Kim et al.	05-2001
5,962,877	Sakurai et al.	10-1999

4,903,117 Okamoto et al. 02-1990

Hitaki Ichii, et al. "Semiconductor Device" Japanese Kokai Patent Application No. HEI 11-284176 (Oct 15, 1999).

Admitted Prior art (Figure 6 in the application).

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al. (USPN 5,962,877) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (USPN 4,903,117).

Sakurai et al. (US reference) discloses a field effect semiconductor device (Fig. 9b) having a semiconductor layer 2 of a first conductivity type (n-type), a collector region 1 of a second conductivity type (p-type) that is formed beneath said semiconductor layer and equipped with a collector electrode 13 on its lower surface, a base region 3 of the second conductivity type that is formed as part of the upper surface of said semiconductor layer, at least one pair of emitter regions 4 of the first conductivity type that are formed as part of the upper surface of said base region, an insulating layer 10 that is formed to contact said base region that is located between said emitter regions

and said semiconductor layer, a gate electrode 11 that is placed on the upper surface of said insulating layer, an interlayer insulating film 14 that is formed to cover said gate electrode, and an emitter electrode 12 that is formed over the interlayer insulating film, base region, and emitter regions. Sakurai et al. does not disclose a barrier metal layer formed to continuously contact said interlayer insulating film, base region, emitter regions, and under said emitter electrode. Sakurai et al. (Japanese reference) discloses a field effect semiconductor device (Fig. 2) comprising a barrier metal layer 21 of molybdenum silicide with a thickness of more than 60 nm formed to continuously contact an interlayer insulating film 12, base region 2, emitter regions 3, and under an emitter electrode 20 of aluminum. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the structure of Sakurai et al. (US reference) by forming the emitter electrode 12 of aluminum and providing a barrier metal layer having a thickness of more than 60 nm as taught by the Sakurai Japanese reference so that the emitter electrode of aluminum provides relatively low resistivity and low cost, and the barrier metal layer continuously contacts said interlayer insulating film, base region, and emitter regions to eliminate silicon residue and prevent aluminum diffusion into the silicon substrate. The modified Sakurai et al. does not disclose the barrier metal layer formed of titanium nitride. Molybdenum silicide and titanium nitride are barrier materials known in the art and routinely used to form barrier metal layer in semiconductor device as shown for example by Okamoto et al. (see Fig. 1 and col. 3, lines 3-15) to prevent spiking in the junction between the emitter electrode and the silicon substrate, to obtain low resistance ohmic contact and

to serve as an excellent diffusion barrier between aluminum and silicon. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable barrier material for the barrier metal layer of the modified Sakurai et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416.

Regarding claim 3, Sakurai et al. (Japanese reference) teaches the thickness of the barrier metal layer is 60 nm.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al. (US 5,962,877) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (US 4,903,117) as applied to claims 1-3 and 5 above, and further in view of Kim et al. (US 6,229,166).

The modified Sakurai et al. does not explicitly disclose the interlayer insulating film 14 having an impurity density less than 5 mol %. Undoped silicon oxide and impurity doped silicon oxide are dielectric materials known in the art and routinely used to form interlayer insulating film in semiconductor device as shown for example by Kim et al. (interlayer insulating film 108, col. 4, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for the interlayer insulating film 14 of the modified Sakurai et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416. Since the

layer 14 is undoped silicon oxide, the impurity density of the interlayer insulating film 14 is inherently less than 5 mol %.

Claims 6-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (USPN 4,903,117).

Admitted Prior art discloses a field effect semiconductor device (Fig. 6 in the application) comprising a semiconductor layer (42, 43) of a first conductivity type (n-type), wherein said semiconductor layer comprises a buffer layer 43 of a first doping concentration and a second layer 42 of a second doping concentration, wherein said first doping concentration is higher than said second doping concentration; a collector region (44, 45) of a second conductivity type (p-type) formed beneath said semiconductor layer and equipped with a collector electrode 45 on its lower surface; a base region 46 of the second conductivity type formed as part of the upper surface of said semiconductor layer; at least one pair of emitter regions 47 of the first conductivity type formed as part of the upper surface of said base region, an insulating layer 48 formed to contact said base region, located between said emitter regions and said semiconductor layer; a gate electrode 49 placed on the upper surface of said insulating layer; an interlayer insulating film 51 formed to cover said gate electrode; and an emitter electrode 53 formed over the interlayer insulating film, base region, and emitter regions. Admitted Prior Art does not disclose the emitter electrode comprising aluminum, and a barrier metal layer formed to continuously contact said interlayer insulating film, base region, emitter regions, and under said emitter electrode. Sakurai

et al. (Japanese reference) discloses a field effect semiconductor device (Fig. 2) comprising a barrier metal layer 21 of molybdenum silicide with a thickness of more than 60 nm formed to continuously contact an interlayer insulating film 12, base region 2, emitter regions 3, and under an emitter electrode 20 of aluminum. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the structure of Admitted Prior Art by forming the emitter electrode 53 of aluminum since aluminum has relatively low resistivity and low cost, and providing a barrier metal layer having a thickness of more than 60 nm as taught by the Sakurai Japanese reference so that the barrier metal layer continuously contacts said interlayer insulating film, base region, and emitter regions in order to eliminate silicon residue and prevent aluminum diffusion into the silicon substrate. The modified APA does not disclose the barrier metal layer formed of titanium nitride. Molybdenum silicide and titanium nitride are barrier materials known in the art and routinely used to form barrier metal layer in semiconductor device as shown for example by Okamoto et al. (see Fig. 1 and col. 3, lines 3-15) to prevent spiking in the junction between the emitter electrode and the silicon substrate, to obtain low resistance ohmic contact and to serve as an excellent diffusion barrier between aluminum and silicon. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable barrier material for the barrier metal layer of the modified Sakurai et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416.

Regarding claim 8, Sakurai et al. (Japanese reference) teaches the thickness of the barrier metal layer is 60 nm.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (US 4,903,117) as applied to claims 6-8 and 10 above, and further in view of Kim et al. (US 6,229,166).

The modified APA as described above does not explicitly disclose the interlayer insulating film 51 having an impurity density less than 5 mol %. Undoped silicon oxide and impurity doped silicon oxide are dielectric materials known in the art and routinely used to form interlayer insulating film in semiconductor device as shown for example by Kim et al. (interlayer insulating film 108, col. 4, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for the interlayer insulating film 51 of the modified APA, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416. Since the layer 51 is undoped silicon oxide, the impurity density of the interlayer insulating film 51 is inherently less than 5 mol %.

(11) Response to Argument

In response to the first issue, appellant states that there is no motivation to combine the teachings of Sakurai, JP '176 and Okamoto. Appellant further states that one of ordinary skill in the art would not have been motivated to combine the non-

aluminum structure of Sakurai with the barrier metal layer of the different structure of JP '176. The examiner respectfully submits that there is no evidence of the record to show that the structure of Sakurai is a non-aluminum structure as alleged by appellant. Sakurai is silent about the material being used for the emitter electrode 12 which cannot be interpreted as a non-aluminum as suggested by appellant. In fact, the emitter electrode 12 could be made of aluminum because aluminum is notoriously known and used widely in the art for its low cost and low resistivity as disclosed by JP '176 (layer 20 as an aluminum emitter electrode). It is also clear in the final office action that motivations have been provided for the combination of the prior art references. If the basis for the argument is that prior art devices are not physically combinable, the examiner respectfully disagrees because it has been held that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, JP '176 clearly teaches emitter electrode of aluminum and a barrier metal layer to eliminate silicon residue and prevent aluminum diffusion into the silicon substrate and Okamoto discloses a barrier metal layer of either titanium nitride or molybdenum silicide to prevent spiking in the junction between the emitter electrode and the silicon substrate, to obtain low resistance ohmic contact and to serve as an excellent diffusion barrier between aluminum and silicon.

In response to appellant's arguments against the references individually as well as no reasonable expectation of success in combining the cited references of distinct structures, the examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Furthermore, the examiner relies only on the use of the barrier metal layer as suggested by JP '176 and the material of titanium nitride for the barrier metal layer as taught by Okamoto for the advantages that a barrier metal layer of titanium nitride provides as disclosed above. It is the examiner's position that if a barrier metal layer works in JP '176 and a barrier metal layer of either titanium nitride or molybdenum silicide could be used effectively in Okamoto, then it would have been obvious to a person having ordinary skill in the art to use a barrier metal layer of titanium nitride in Sakurai reference for the reasons as described above. Appellant's argument does not hold since it cannot replace evidence when evidence is necessary.

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., having a greater amount of breakdown withstanding on lines 1-2 of page 9 of the appeal Brief) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to the second issue, appellant states that there is no suggestion or motivation to combine the teachings of Sakurai, JP '176, Okamoto and Kim, and no reasonable expectation of success in the combination of the references. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, JP '176 clearly teaches emitter electrode of aluminum and a barrier metal layer to eliminate silicon residue and prevent aluminum diffusion into the silicon substrate; Okamoto discloses a barrier metal layer of either titanium nitride or molybdenum silicide to prevent spiking in the junction between the emitter electrode and the silicon substrate, to obtain low resistance ohmic contact and to serve as an excellent diffusion barrier between aluminum and silicon; and Kim teaches using undoped silicon oxide layer 14 as an interlayer insulating film wherein the impurity density of the interlayer insulating film 14 is inherently less than 5 mol %.

In response to appellant's arguments against the references individually as well as no reasonable expectation of success in combining the cited references of distinct structures, the examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Furthermore, the examiner relies only on the use of an undoped silicon oxide layer as suggested by Kim for the interlayer insulating film 14 of Sakurai since the combination of Sakurai, JP '176 and Okamoto disclose all the features of the claimed structure except for the material of the interlayer insulating film. Furthermore, appellant's argument that there is no reasonable expectation of success does not hold since it cannot replace evidence when evidence is necessary.

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., having a greater amount of breakdown withstanding on lines 15-16 of page 10 of the appeal Brief or improving the characteristics of an IGBT on line 21 of page 10 of the Appeal Brief) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to the third issue and fourth issue, Appellant states that the teaching or suggestion must be found in the prior art, not in Appellants' disclosure. As a result, the combination of Figure 6, JP '176, Okamoto and Kim is improper. The examiner

respectfully disagrees with the remark. MPEP 2129 clearly states that admissions by applicant constitute prior art. When something is stated as prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejections. In re Nomiya, 509 F.2d 566, 184 USPQ 607, *>611< (CCPA 1975). In page 1 and page 6 of the disclosure, Appellant clearly states Figure 6 is a structure of a conventional IGBT. Therefore, Figure 6 is taken as prior art and can be used in obviousness rejection. Therefore, the combination of the prior art references is proper.

In conclusion, it is respectfully submitted that a prima facie case of obviousness has been established and Appellants have failed to rebut.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thien Tran
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PATENT EXAMINER

tt
October 9, 2003

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